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13. ABSTRACT (Maximum 200 words) The purpose of this AASERT grant was to extend the work on resonant tunneling devices to include a new structure which has shown evidence of zero-bias memory switching and multi-state behavior. This device is known as a quantum storage device, or QSD. This device features a triple barrier resonant tunneling device, yielding a three terminal device. Under the AASERT, extensive simulations were performed using the Schrodinger-Poisson and Wigner formalisms. Optimization of the QSD design to achieve high on-off resistance ratios is a main focus of the parameter study. Results to date will be described.					
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Multi-State Quantum Storage Devices

technical contact:

Dean P. Neikirk

Department of Electrical and Computer Engineering

The University of Texas at Austin

Austin, TX 78712

phone: (512) 471-4669

FAX: (512) 471-5445

e-mail: neikirk@mail.utexas.edu

Objectives

The purpose of this AASERT grant was to extend our work on resonant tunneling devices to include a new structure which has shown evidence of zero-bias memory switching and multi-state behavior. We refer to this device as a quantum storage device, or QSD. The QSD is a modified quantum well diode that relies on the interaction of a quantum well region with a $N/N^+/N$ (see Figure 1) doped region to achieve its multiple conduction states. Unlike other multiple state quantum structures, we have found that the QSD has different current versus voltage curves corresponding to the different conduction states, even at zero bias (Figure 2). Experimental findings indicate that these states remain stable even under short circuit conditions and can only be switched from one state to another with the application of bias in excess of certain threshold voltages. Several quantum models developed by our group have been used to investigate QSD device design.

Status of Effort

New developments on resonant tunneling diode memory switching devices that should enhance application in ultra-dense memory and logic have been made. The original device (Fig. 1), a double barrier resonant tunneling diode in the GaAs/AlAs materials system has shown multiple conduction states and memory switching in Schrödinger-Poisson (Fig. 3) and Wigner formalism simulations, as well as in laboratory measurements (Fig. 2). In new work we have demonstrated this phenomenon in similarly designed triple barrier resonant tunneling devices in Schrödinger-Poisson simulations and in the laboratory. Memory switching has not been previously reported in these devices. The triple barrier device is part of our development of a three terminal quantum storage device which we believe will have significantly enhanced switching characteristics. The additional AlAs layer has been used as an etch stop in the fabrication of three terminal devices. A process has been developed using a succinic acid selective etch to etch down to the top AlAs layer where metal is evaporated directly on the N^+ layer, forming a Schottky

contact. We have also completed a two-dimensional Schrödinger-Poisson simulator to facilitate design of the three terminal devices.

Description of student research (8/93 - 8/94)

There are several problems that must be solved before the QSD can become a practical memory device. Since the key to changing the state is to change the potential at the N^+ layer an efficient way of changing this potential must be developed. The method of switching in two terminal QSDs used in past experiments has been the application of a high bias across the contacts; this has proved to be problematic, however. Hit/miss ratios (i.e., single pulse switching probability) are on the order of 2 and switching power is very high (about 0.1W). This is believed to be because the dynamics of switching by application of a bias voltages on the two terminal device are unfavorable. One solution to this problem is make a three terminal device where the third or write terminal is in direct contact with the N^+ layer.

The challenge in fabricating a three-terminal QSD is the difficulty in reproducibly (and independently) contacting the extremely thin ($\sim 100 \text{ \AA}$) heavily doped spacer layer. To fabricate such a device, an etch-down of approximately 5000 \AA to the N^+ layer is first required. This etch-back, however, must stop with an accuracy of less than 100 \AA . At this point, the exposed surface, which constitutes the "base," must be contacted by a metallurgy that does not spike through the thin spacer layers or quantum well, thereby shorting the device. One fabrication process for placing a contact on the thin N^+ layer involves placing a thin etch stop layer (AlAs in this case) above it, and using a selective etch, as shown in Fig. 4. Several issues that must be addressed during such a process are the etch selectivity, the "base" contact resistance due to surface depletion, non-alloyed contact formation, and the process reproducibility. The use of a succinic acid solution to selectively etch down to the thin AlAs etch stop [Tang, 1993 #24] shown in Fig. 4 has been successfully demonstrated under the sponsorship of this grant.

The original QSD was a double barrier resonant tunneling diode (DBRTD) but because of the presence of this etch stop layer the new device is a triple barrier resonant tunneling diode

(TBRTD), with one of the quantum wells heavily doped. The cross section of a three terminal device is shown in Fig. 4. To fabricate the central mesa of this device a TBRTD sample is patterned with positive photoresist. Ni/AuGe/Ni contacts are thermally evaporated onto the surface and liftoff is performed. Central mesa sizes down to the 1-2 μm range have been made. Because ohmic contacts are desired at the central mesa a rapid thermal anneal (RTA) of 400°C for 30 seconds is done. Next the central mesa is isolated down to the N^+ layer. A $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$, 8:1:1 etch is done at room temperature for 10 seconds to etch away any oxidized GaAs at the surface. Succinic acid is used to etch down to the first AlAs layer [Tang, 1993 #24]. The etch rate is about 1000 $\text{\AA}/\text{minute}$ and the selectivity is greater than 500. The final control on the etch is by visual inspection. The surface becomes rough and colored during the etch but is mirror-like when the etch halts at the etch stop's planar surface. We expect the 6 ML etch stop to contain the etch for several minutes. Finally, a self aligned process was used to evaporate a gate onto the exposed surface contacting the N^+ layer.

For the TBRTD structure grown, Schrödinger-Poisson self-consistent current density vs. bias curves are shown in Figs. 5 and 6. Figure 5b is a more detailed view of the low bias region in Fig. 5. As in the DBRTD based device, there are two separate current density vs. bias curves passing through zero bias. The electron concentrations for these two states at zero bias are shown in Fig. 6. Both states are space charge neutral, but the difference in electron concentration is greatest, about $1.1 \cdot 10^{18} \text{ cm}^{-3}$, in the N^+ layer. Again, as in the DBRTD QSDs, the high current state has a low electron concentration in the N^+ layer. There is no assurance that these are the only two stable states. The observation of two states is taken as a demonstration of existence, but not an indication of the extent, of the bias range over which these states may be stable. Peaks in current are observed at about 0.4, -0.06, 0.025, 0.1, and 0.42 volts in this simulation.

Preliminary experimental measurements for these devices also show two I-V curves, as shown in Fig. 7. These I-V curves show hysteresis due to space charge effects. Flexures in these I-V curves occur at approximately -0.9, -0.4, 0.2, and 0.6 volts. For the high current state current peaks are at 0.046 amps were observed in the simulation and 0.038 amps in the lab measurements.

To simulate the behavior of the three terminal device, the contact at the N^+ layer represents an additional boundary condition. A significant amount of our effort in the last year has been in the development of a 2-D Schrödinger - Poisson algorithm. This algorithm uses a finite difference matrix implementation of the quantum transmitting boundary method (QTBM) to determine the bound and unbound electron concentration, which it iterates with Poisson's equation. The bound state concentration is determined by solving the effective mass equation for its eigenvalues. A Lanczos algorithm is used to tridiagonalize the matrix and then an LR algorithm is used to determine the eigenvalues. These are refined using a Newton Raphson iteration. Eigenvectors are determined using inverse iteration with known the eigenvalues. This algorithm has been tested successfully for real, symmetric and complex, non-symmetric matrices. The algorithm may also be used to calculate transmission coefficients from which currents will be determined.

The unbound carrier concentration is determined by integrating the density of states over energy. This involves solving the Schrödinger boundary value problem at each energy, which may done by direct LU decomposition or iterative solution. Our algorithm has been implemented entirely in the Sparse data structure. This is an orthogonal link list that allows efficient storage of sparse matrices. It also facilitates solution by LU decomposition. This is done very efficiently and growth of the sparse matrix during solution is minimized.

Since energies in the numerical integration are very close together preconditioned conjugate gradient techniques have been tried. The solution at each energy is assumed to be a small perturbation of the solution at the last energy. This has potential to be the fastest method of solution with lowest memory requirements, only a few times the size of the solution vector. At the present time the matrix realization of the problem appears to be too ill conditioned for the iterative solution techniques that have been attempted to solve the problem more efficiently than the LU decomposition. We are continuing to test and evaluate this algorithm. Preliminary results of a two-dimensional self-consistent solution for the coupled Schrödinger-Poisson equations are shown in Fig. 8. We have again seen evidence of two solutions, although the addition boundaries on the

two sides of the device do have a strong influence on convergence, and it is not yet clear whether multiple solutions of comparable numerical significance exist in the simulations.

A three terminal device would be functionally similar to an asynchronous D type flip-flop. A simple resistive model for its operation is shown in Fig. 9. If we require that the input and output of such a device be self compatible (i.e., the output should be sufficient to drive the "write" terminal on the next device) then the required ratio of the resistances produced by the two states of the QSD can be determined. Figure 10 shows the voltage difference (from the supply or "rail" voltages) produced by the two states as a function of the ratio of their resistances. This indicates we must achieve a ratio greater than five, but preferably at least ten, to have well separated on and off voltages at the "read" terminal. There does not seem to be significant advantage to ratios greater than about 40. Optimization our QSD design to achieve such high on-off resistance ratios is a main focus of our parameter study. Preliminary model results have shown QSD structures can produce resistance ratios as high as 60.

In summary, under the sponsorship of this grant, we have continued to make strides in the development of quantum storage devices in the areas of modeling, growth, fabrication, and device characterization. These developments must proceed hand-in-hand for reliable results to be achieved. In addition we have attempted to consider potential practical application of this device at every stage.

Personnel Supported

During this grant two different graduate research students were supported through this program. During the first year of the grant Mr. (now Dr.) Jason Lewis was supported; subsequently Mr. Olin Hartin was supported. Dr. Lewis, in collaboration with Dr. K. K. Gullapalli, used three dimensional thermal modeling to insure that temperature rises within our small, high current density devices were small enough to insure that the memory switching effect experimentally observed was not an artifact of heating damage. Mr. Hartin is currently working on a two-dimensional quantum transport model, as well as fabricating and testing the triple barrier RTDs. Mr. Hartin has performed a large set of experiments, including:

- succinic acid etching for selective removal of GaAs relative to AlAs
- AlAs oxidation experiments in thin barrier resonant tunneling structures
- non-alloyed Pd/Ge contacts for use in three terminal QSDs

He has also developed several new Schrödinger/Poisson simulation tools for use in QSD design and analysis, including:

- revised one-dimensional Schrödinger/Poisson simulator
- two-dimensional Schrödinger/Poisson simulator

Mr. Hartin should complete his PhD during the summer of 1997.

Publicatlons supported in whole or part by this grant:

Refereed Journal Publications:

K. K. Gullapalli, D. R. Miller, and D. P. Neikirk, "Simulation of quantum transport in memory-switching double-barrier quantum-well diodes," **Phys. Rev. B (Condensed Matter)** 49, 15 January 1994, pp. 2622-2628.

Refereed Conference Proceedings:

K. K. Gullapalli and D. P. Neikirk, "Incorporating spatially varying effective-mass in the Wigner-Poisson model for AlAs/GaAs resonant-tunneling diodes," Proceedings of the Third Annual International Workshop on Computational Electronics, Portland, OR, May 18-20, 1994, pp. 171-174.

O. Hartin, D. P. Neikirk, A. Anselm, and B. Streetman, "Three Terminal Quantum Storage Device," AVS 14th Annual Symposium on Electronic Materials, Processing, and Characterization, Austin, Texas, USA, June 6-7, 1995.

O. Hartin, D. P. Neikirk, A. Anselm, and B. Streetman, "Design and Fabrication of a Three Terminal Quantum Storage Device," 1995 IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Cornell University, Ithaca, NY, USA, August 7-9, 1995, pp. 4.15.

Dissertations:

Jason Lewis, "Far-Infrared and Sub-Millimeter Microbolometer Detectors," University of Texas at Austin, May, 1994.

Kiran Kumar Gullapalli, "Heterostructure Device Simulation using the Wigner Function," University of Texas at Austin, Aug. 1994.

Discoveries/Inventions/Patent Disclosures

There were no new inventions under this grant.

References

[1] A. J. Tang, K. Sadra, and B. G. Streetman, "Selective Etching of $\text{Al}_x\text{Ga}(1-x)\text{As}$ and $\text{In}(\text{Al}_x\text{Ga}(1-x))\text{As}$ Alloys in Succinic Acid-Hydrogen Peroxide Solutions," *Journal of the Electrochemical Society*, vol. 140, pp. 82-83, 1993.

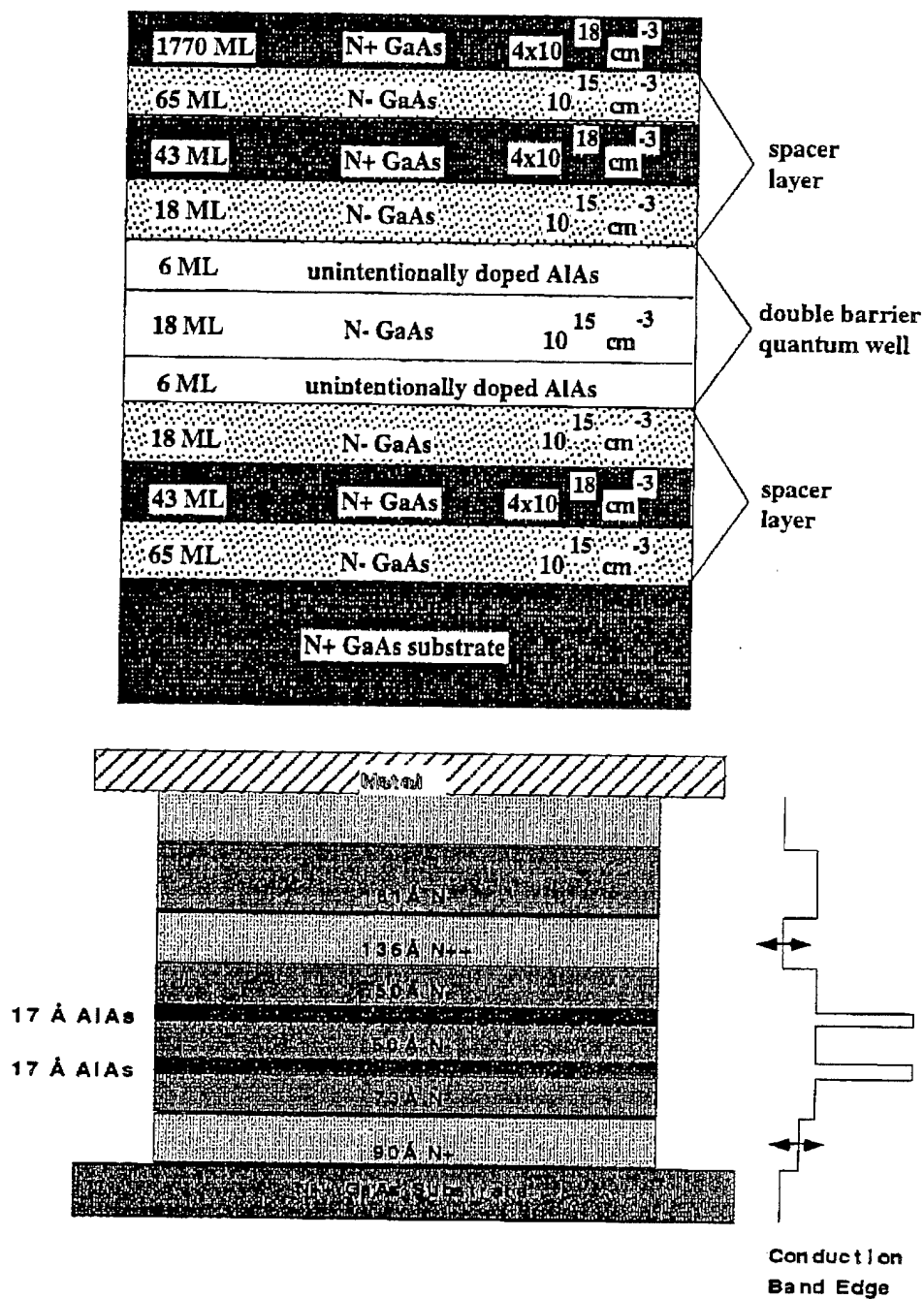
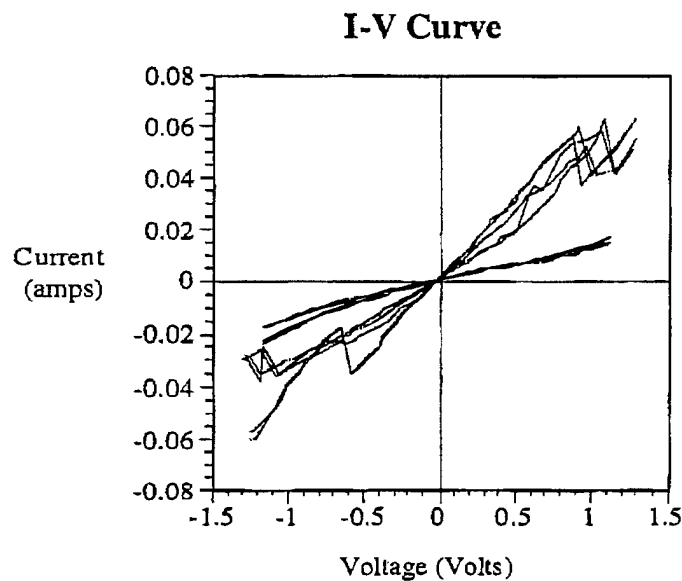
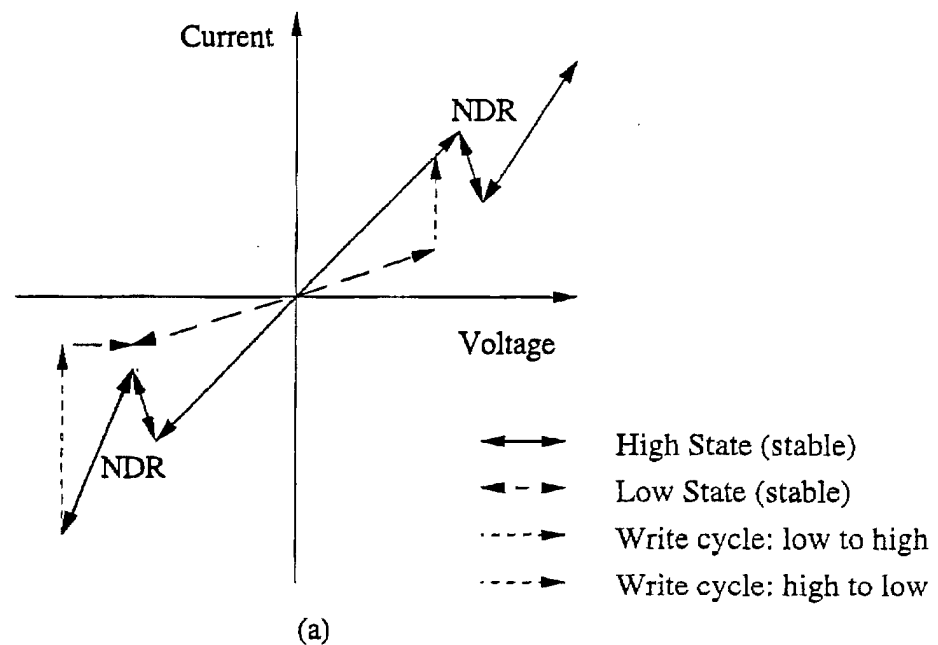


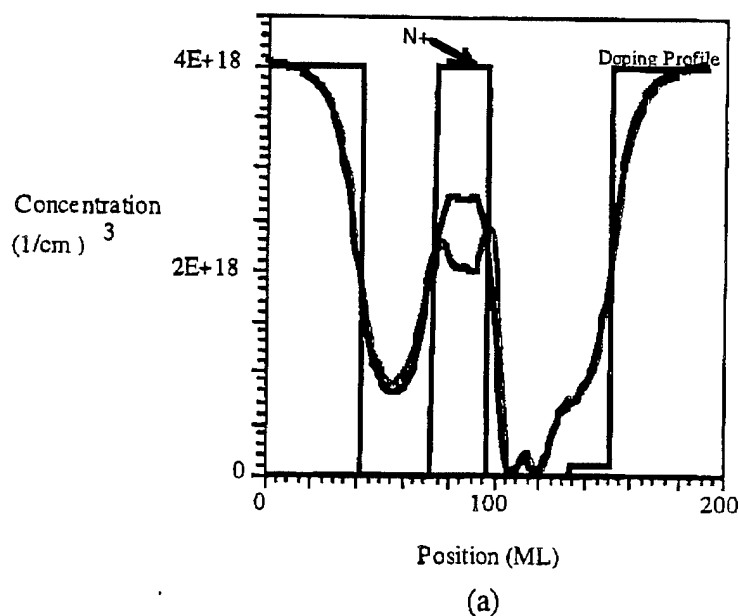
Figure 1: Multi-state device using a symmetric N-/N⁺/N- spacer layer / AlAs barrier / GaAs quantum well / AlAs barrier / N-/N⁺/N- spacer layer structure.



(b)

Figure 2: (a) Schematic diagram indicating the switching and stable operating regions of the multi-state $N^-/N^+/N^-$ spacer layer / AlAs / GaAs quantum well device shown in Fig. 1. (b) Laboratory measured I-V curves showing multiple states. There are two high current states and one low current state.

Electron Concentration vs. Position



Current Density vs. Bias Voltage

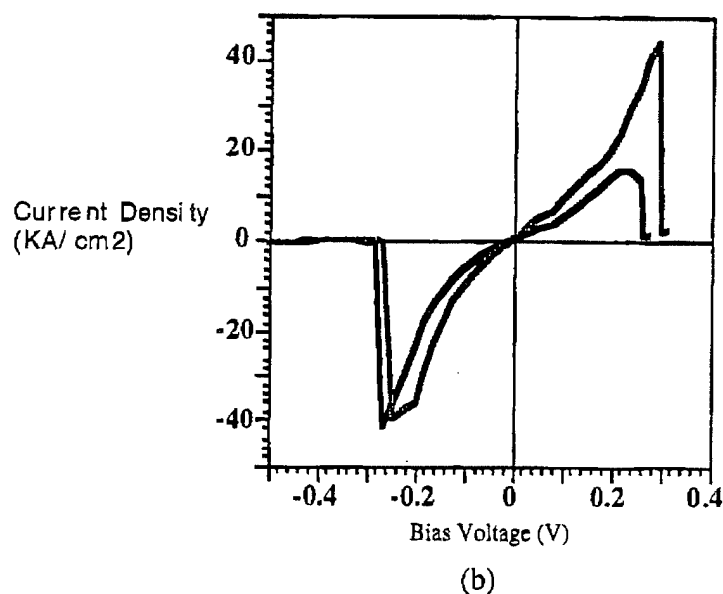


Figure 3: Schrödinger-Poisson simulation results: (a) The square black curve is the doping profile. The black curve is the equilibrium electron concentration in the low current state and the gray curve is the electron concentration of the high current state from figure 2. (b) Schrödinger-Poisson simulated current density vs. bias curves of the two conduction states of the device in Fig. 1.

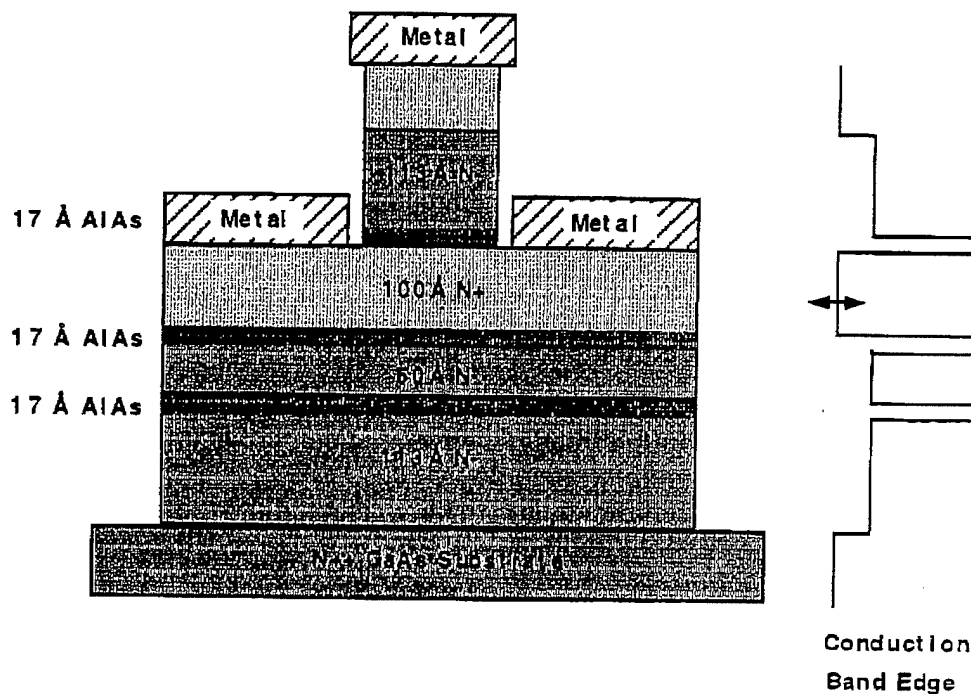
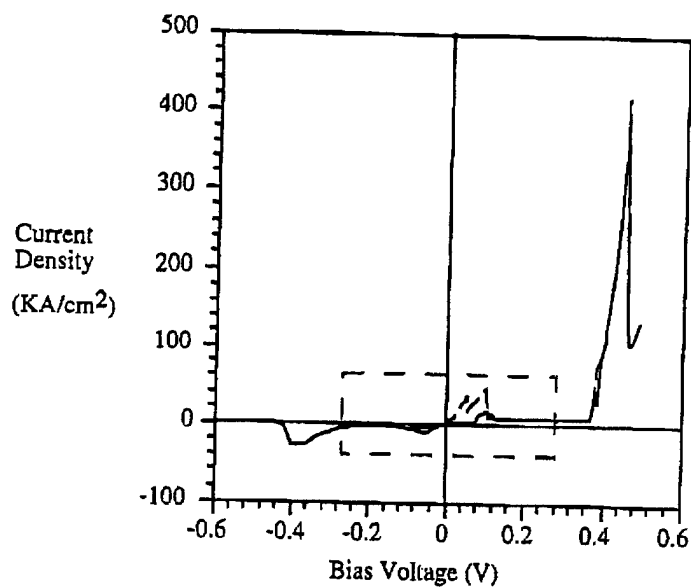


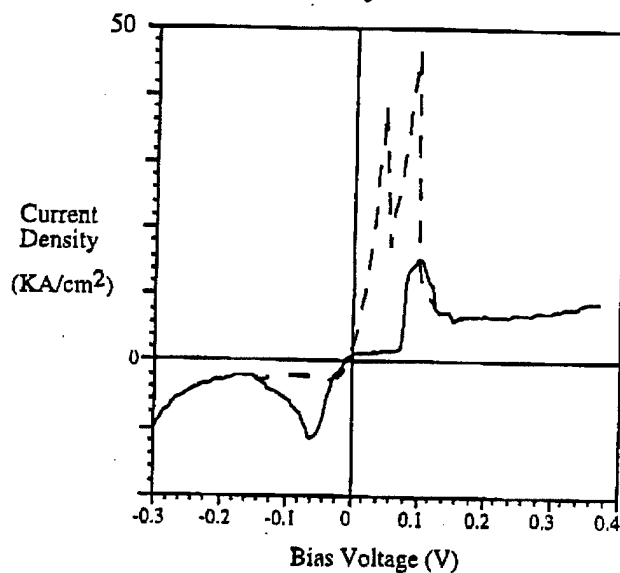
Figure 4: Structure of a three terminal device after the fabrication process described, similar to that shown in Fig. 1.

Current Density vs. Bias Curves



(a)

Inset Region Current Density vs. Bias Curves



(b)

Figure 5: Current density vs. bias voltage from Schrödinger-Poisson modeling of the structure in Fig. 4. The region in the box is expanded in (b).

Electron Concentration vs. Position

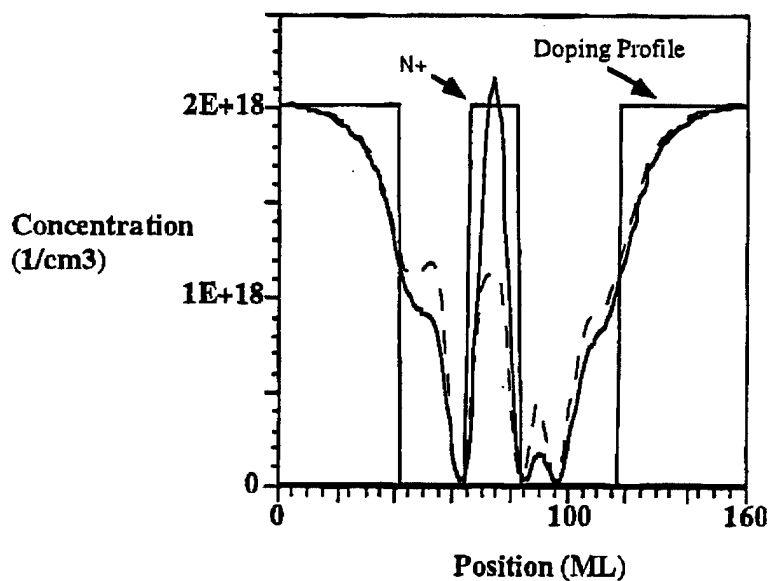


Figure 6: Equilibrium electron concentration from Schrödinger-Poisson models of the structure in Fig. 4.

I-V Curve

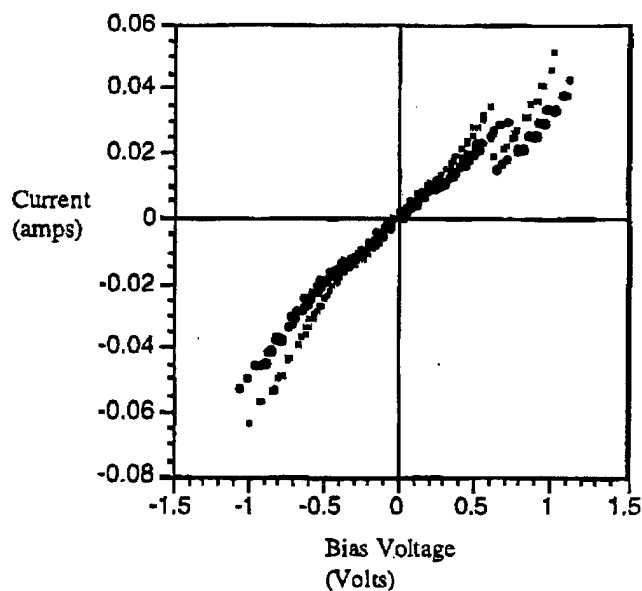


Figure 7: I-V curves from laboratory measurements of the structure in Fig. 4.

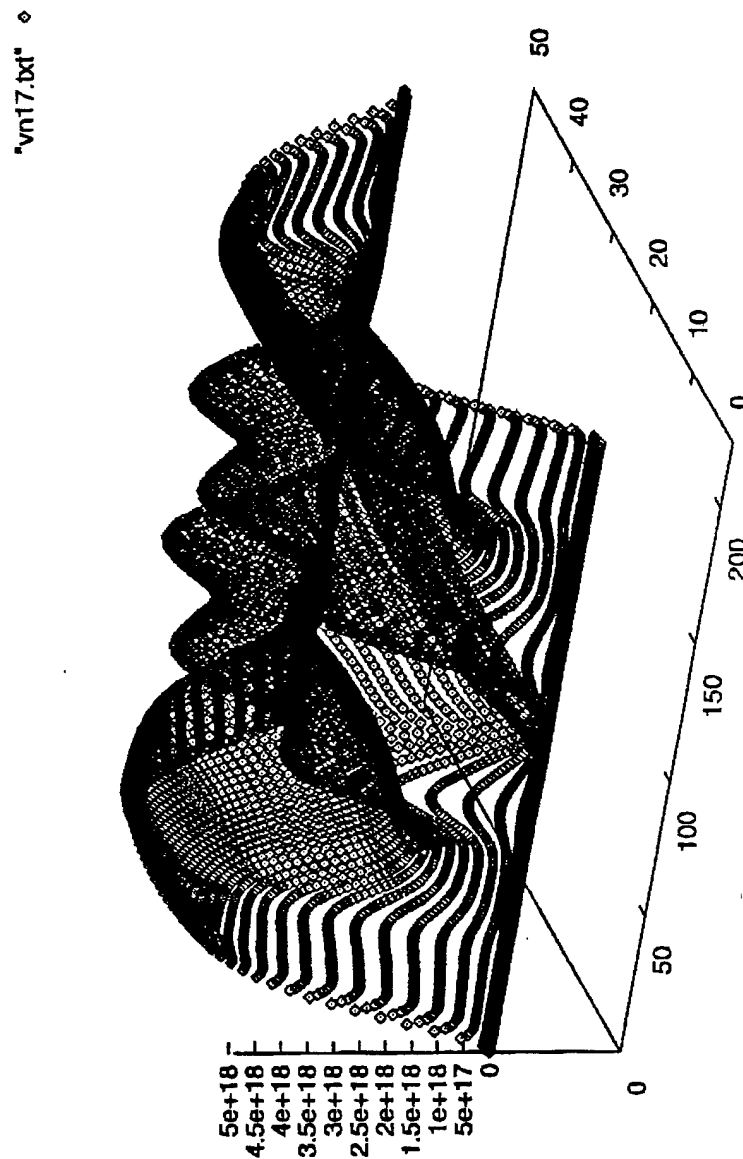


Figure 8: Preliminary two-dimensional simulation results for a QSD similar to that shown in Fig.

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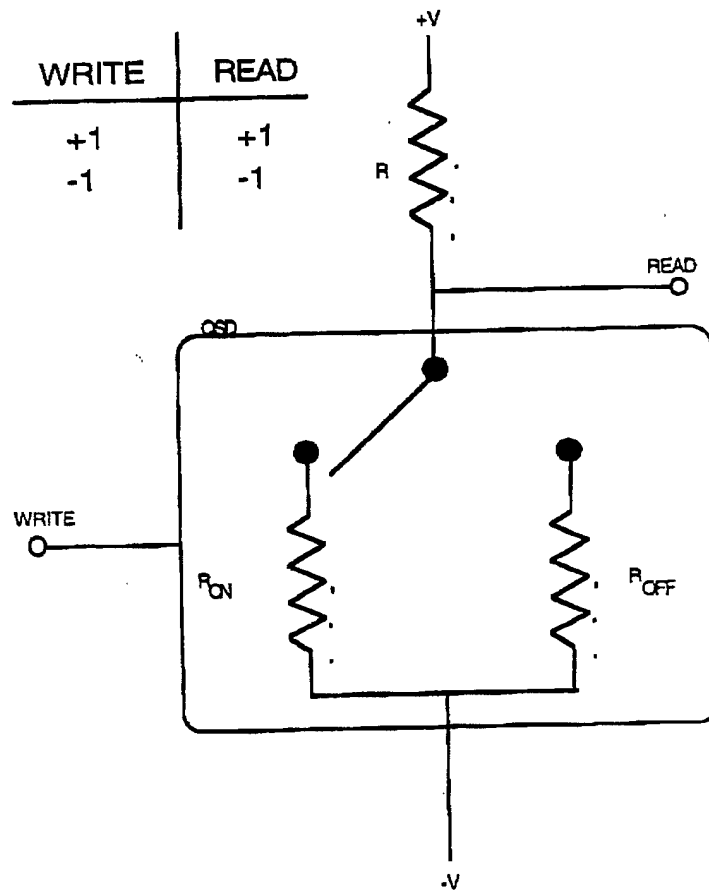


Figure 9: Resistor model of a QSD-based D flip-flop. The write terminal controls the state shown here by the position of the switch. The truth table shows operation at the READ and WRITE terminals of the flip-flop. The resistance R is determined by R_{on} and R_{off} .

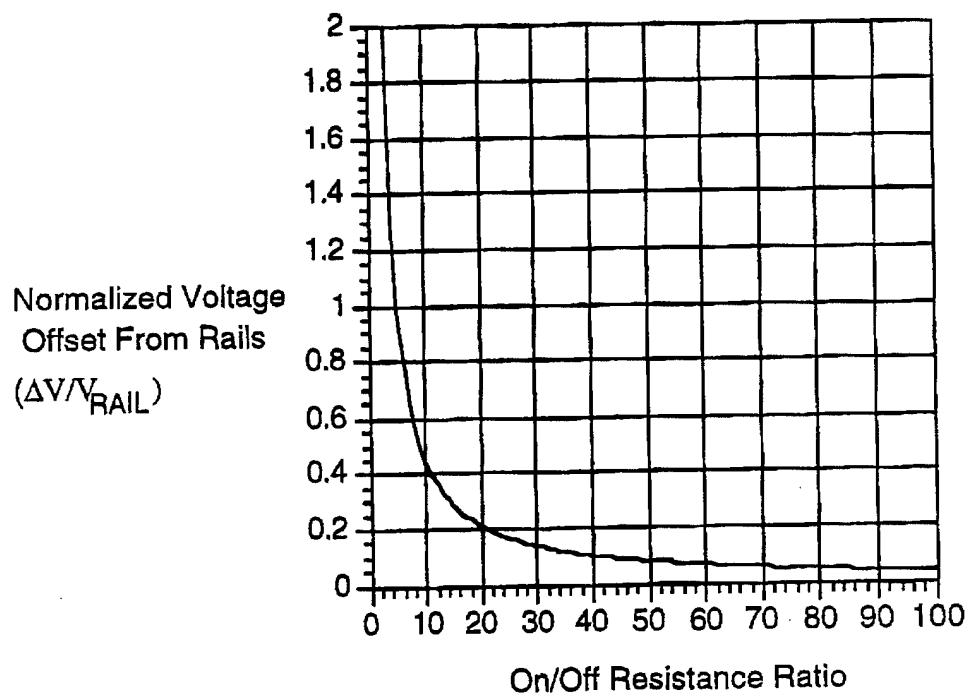
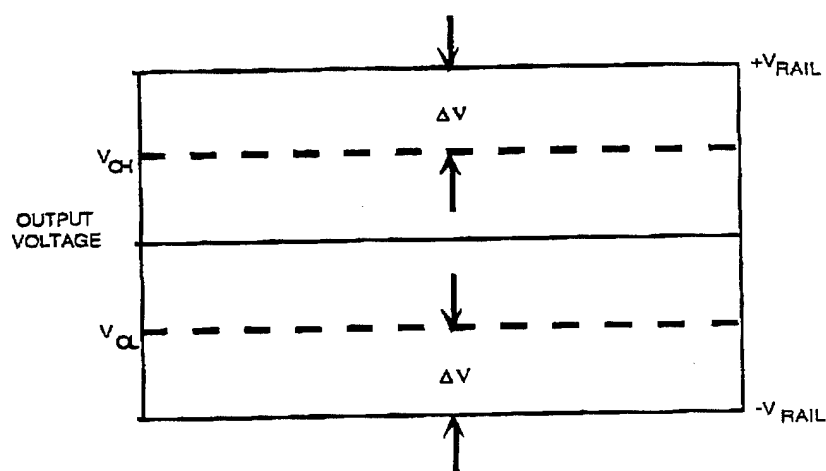


Figure 10: Normalized output voltage as a function of on/off resistance ratio. This is based on the D flip-flop implementation shown in Figure 9.